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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/071,348 | 02/08/2002 | Daniel R. Meacham | P04986 | 2784 |

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| EXAMINER | |
|---|---|
| COX, CASSANDRA F | |
| **ART UNIT** | **PAPER NUMBER** |
| 2816 | |

DATE MAILED: 04/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/071,348 | MEACHAM ET AL. | |
| | Examiner | Art Unit | |
| | Cassandra Cox | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 January 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

Applicant's arguments filed 01/13/04 have been fully considered but they are not persuasive. The rejection has been restated below to more clearly point out the capability of the circuit to use current control for the delay lines.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7 and 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Notani et al. (U.S. Patent No. 6,396,888).

In reference to claim 1, Notani discloses in Figure 18 a circuit having a first current controlled delay line (7N; see column 20, lines 44-48 where Notani discloses that the delay lines may also be current controlled as called for in the claims) capable of receiving an FSK signal (CKFPN) and delaying the FSK signal (CKFPN) by a desired time delay to thereby produce a time-delayed FSK signal (RCKN); a first multiplier (OGN) capable of receiving and multiplying the FSK signal (CKFPN) and the time-delayed FSK (DCKFPN) signal to thereby produce an output product signal (RCKN) proportional to a phase shift between the FSK signal and the time-delayed FSK signal and a delay locked loop comprising a second current controlled delay line (71) substantially similar to the first current controlled delay line (7N), wherein the delay

locked loop receives a reference clock signal (CKFP1) having a time period equal to the desired time delay and adjusts a control current level in the second current controlled delay line (71) until a delay of the second current controlled delay line (71) matches the time period of the reference clock signal, wherein the control current level is then used to adjust a delay of the first current controlled delay line (7N). Notani does not disclose that the signal (CKFPN) is an FSK signal, however it is well known in the art the delay lines can be used to delay a number of different types of signals including FSK signals, of which fact official notice is taken. It would have been obvious to one skilled in the art at the time of the invention that the delay line (7N) of Notani could be used to delay an FSK signal as well as any other type of signal. This requirement is seen to be a design expedient dependent on the particular environment and the desired outcome. The same applies to claim 15.

In reference to claim 2, Notani discloses in column 20, lines 44-48 that the second controlled delay line can be controlled by adjusting its bias current. The same applies to claims 3, 16, and 17.

In reference to claim 4, Notani discloses in Figure 18 that the delay locked loop comprises a phase detector (4) having a first input for receiving the reference clock signal (CKFP1) and a second input for receiving an output signal (DCKFP1) of the second current controlled delay line (71) and generating a correction control signal (Vb) determined by a phase difference between the reference clock signal (CKFP1) and the output signal (DCKFP1) of the second current controlled delay line (71). The same applies to claim 18.

In reference to claim 5, Notani discloses in Figure 20 that the second current controlled delay line may also be configured as an oscillator (8). The same applies to claim 19.

In reference to claim 6, Notani discloses in Figure 18 a circuit further comprising: a third current controlled delay line (7(N-1)) capable of receiving an FSK signal (CKFP(N-1)) and delaying the FSK signal (CKFP(N-1)) by a desired time delay to thereby produce a time-delayed FSK signal (RCK(N-1)); and a second multiplier (OG(N-1)) capable of receiving and multiplying the FSK signal (CKFP(N-1)) and the time-delayed FSK (DCKFP(N-1)) signal to thereby produce an output product signal (RCK(N-1)) proportional to a phase shift between the FSK signal and the time-delayed FSK signal; wherein the delay locked loop uses the control current level to adjust a delay of the third current controlled delay line (7(N-1)), see column 18, lines 25-30. The same applies to claims 7, 20, and 21.

3. Claims 8-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Notani et al. (U.S. Patent No. 6,396,888) in view of Bagby (U.S. Patent No. 5,319,679).

In reference to claim 8, Notani discloses all the limitations of the claim as mentioned above with respect to claims 1 and 15, except Notani does not disclose demodulation circuitry capable of receiving an incoming radio frequency (RF) signal and generating therefrom a frequency-shift keyed (FSK) signal having a nominal frequency, f. Bagby discloses in Figure 1, demodulation circuitry (20, 21) capable of receiving an incoming radio frequency (RF) signal (14) and generating therefrom a frequency-shift keyed (FSK) signal (which is seen to be the output of block 21) having a nominal

frequency, f (see column 3, lines 20-26 and 49-59). Since it is obvious that the signal being delayed in the Notani circuit would have to be generated in some method, any circuit capable of generating a signal capable of being delayed would be suitable to provide the signal input to the delay line (7N) of Notani. Therefore, it would have been obvious to one skilled in the art at the time of the invention that the frequency shift keyed signal produced by Bagby could be provided as the signal to be delayed by the circuit of Notani.

In reference to claim 9, Notani discloses in column 20, lines 44-48 that the second controlled delay line can be controlled by adjusting its bias current. The same applies to claim 10.

In reference to claim 11, Notani discloses in Figure 18 that the delay locked loop comprises a phase detector (4) having a first input for receiving the reference clock signal (CKFP1) and a second input for receiving an output signal (DCKFP1) of the second current controlled delay line (71) and generating a correction control signal (Vb) determined by a phase difference between the reference clock signal (CKFP1) and the output signal (DCKFP1) of the second current controlled delay line (71).

In reference to claim 12, Notani discloses in Figure 20 that the second current controlled delay line may also be configured as an oscillator (8).

In reference to claim 13, Notani discloses in Figure 18 a circuit further comprising: a third current controlled delay line (7(N-1)) capable of receiving an FSK signal (CKFP(N-1)) and delaying the FSK signal (CKFP(N-1)) by a desired time delay to thereby produce a time-delayed FSK signal (RCK(N-1)); and a second multiplier (OG(N-

1)) capable of receiving and multiplying the FSK signal (CKFP(N-1)) and the time-delayed FSK (DCKFP(N-1)) signal to thereby produce an output product signal (RCK(N-1)) proportional to a phase shift between the FSK signal and the time-delayed FSK signal; wherein the delay locked loop uses the control current level to adjust a delay of the third current controlled delay line (7(N-1)), see column 18, lines 25-30. The same applies to claim 14.

***Response to Arguments***

In response to the applicant's arguments filed on 01/13/04, the examiner has restated the rejection to more clearly point out the capability of the circuit to use current control for the delay lines. In addition the examiner does not find persuasive the applicant's argument that the OR gate does not "produce an output product signal proportional to a phase shift" between the signals. It is the examiner's belief that the OR gate is capable of producing an output product between the signals and that the output product signal being proportional to a phase shift between those signals would be an inherent part of that output product signal. This fact is further supported by Kim et al (U.S. Patent No. 6,295,328) which the examiner cites to show that it is well known in the art that OR gates can be used to produce multiplied outputs between two signals (see Figure 3 and column 4, lines 30-36).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-

1741. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM and on alternate Fridays from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

CC

April 18, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800